REMARKS

Claims 1, 4-14, 17-20, 22-27, and 34 were pending in the present application. Claims 4-7, 10, 11, and 34 have been cancelled. Claims 1, 8, and 19 have been amended. Accordingly, claims 1, 8, 9, 12-14, 17-20, and 22-27 are now pending in the application.

Claims 1, 3-14, 17-20, 22-27, and 34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gharachorloo, et al. (U.S. Patent Application Publication Number 2002/0124144) (hereinafter "Gharachorloo") in view of Singhal, et al. (U.S. Patent Number 5,978,874) (hereinafter "Singhal"), and in further view of Van Doren et al. (U.S. Patent No. 6,209,065) (hereinafter "Van Doren"). Although Applicant respectfully traverses portions of this rejection, Applicant has amended the claims to expedite allowance.

Applicant's claim 1, as amended, recites a system comprising in pertinent part

"wherein the address packet and the data packet are part of a read-to-own transaction initiated by the processing subsystem;

wherein the interface in the node is configured to delay providing the data packet on the data network until the interface receives an indication that shared copies of the coherency unit in the additional node have been invalidated;

wherein in response to receiving the address packet via the address network, a **memory subsystem** included in the node is configured to send a data packet indicating the read-to-own transaction to the interface, wherein the interface is configured to forward a read-to-own message on the inter-node network in response to receiving the data packet indicating the read-to-own transaction; and

wherein the additional interface is configured to receive the read-to-own message via the inter-node network and to responsively send an invalidating address packet on the additional address network, wherein in response to the additional processing subsystem having an access right to but not an ownership responsibility for the coherency unit, the additional processing

subsystem is configured to transition its access right to the coherency unit in response to the invalidating address packet."

In regard to the rejection of claim 10, the Examiner points to an output queue 162 as being Applicant's claimed memory subsystem. Applicant respectfully disagrees with the broad of an interpretation by the Examiner. An output queue is nothing more than a buffer.

The above notwithstanding, in the rejection of claim 11 the Examiner acknowledges that Gharachorloo does not teach the limitations of lines 4-6 of the claim and asserts "the Examiner has shown that an access right to a memory line is obtained after gaining ownership; therefore, it can be seen that a processing subsystem may never have an access right to not ownership responsibility for a memory line." However the Examiner indicated that "the limitation is drafted in the alternative; and therefore may not necessarily occur with regards to Applicant's claimed invention, the limitation is met by Gharachorloo."

Applicant has amended claim 1 to include the limitation previously recited in claim 11. However, Applicant has redrafted that limitation to remove the alternative language. Accordingly, Applicant submits neither Gharachorloo nor the other references, teach or suggest "wherein the additional interface is configured to receive the read-to-own message via the inter-node network and to responsively send an invalidating address packet on the additional address network, wherein **in response to** the additional processing subsystem having an access right to but not an ownership responsibility for the coherency unit, the additional processing subsystem is configured to transition its access right to the coherency unit in response to the invalidating address packet," as recited in Applicant's claim 1.

Thus, Applicant submits claim 1, along with its dependent claims patentably distinguishes over the cited references for the reasons given above.

Applicant's claim 19 recites features that are similar to the features recited in claim 1. Accordingly, for at least the reasons given above, Applicant submits claim 19, along with its respective dependent claims patentably distinguishes over the cited references.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-00201/SJC.

Respectfully submitted,

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